

PAT-NO: JP402204848A
DOCUMENT-IDENTIFIER: JP 02204848 A
TITLE: COMPUTER EQUIPMENT FOR ADOPTING ADDRESS TRANSLATION

PUBN-DATE: August 14, 1990

INVENTOR-INFORMATION:

NAME	COUNTRY
IWATA, YOSHIHIRO	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	N/A

APPL-NO: JP01024012
APPL-DATE: February 3, 1989

INT-CL (IPC): G06F012/10

ABSTRACT:

PURPOSE: To constitute a physical cache having a large capacity without increasing a cache access time by providing a translation predicting means and a translation holding means, and updating the translation predicting means by an appropriate condition.

CONSTITUTION: A translation holding means 160 decides whether a physical address which translates an indirect address part of a logical address designated immediately before by a processor 100 by using the logical address designated by the processor 100 is effective or not. In the case when the address is not effective, the processor suspends or extends or retries an access. In this case, a translation support means 150 translates the present logical address and outputs a translated physical address from a translation address output line 151. At that time, a translation predicting means 130 updates a predictive physical address of an entry corresponding to a logical address before by one to the translated physical address, and updates a value of the corresponding logical address indirect address part to the present logical address. In such a way, a physical cache having a larger capacity than a page size can be constituted without increasing a cache access time.

COPYRIGHT: (C)1990,JPO&Japio